IN THE SPECIFICATION

The Examiner objected to informalities in the specification. Please amend the paragraph at page 12, lines 15-28 to address the informalities.

Figure 4 is a diagrammatic representation of a dual return path architecture for implementing adaptive equalization. An input delay line 423 includes a plurality of delay elements 411, 413, 415, etc. Any line including a plurality of elements for shifting an input signal is referred to herein as an input delay line. The input delay line 423 provides intermediate signals to output delay lines 421 and 425. Any line including a plurality of elements for shifting a signal in order to provide either an output signal or a gradient vector is herein referred to as an output delay line. The output delay line 425 includes coefficient multipliers 431, 433, 439, etc. Intermediate signals are provided from input delay line 423 to the coefficient multipliers of output delay lines 425. The intermediate signals multiplied by the coefficient multipliers are then combined with other intermediate signals multiplied by other coefficient multipliers to yield an output signal y_k ~~411~~ 441. According to various embodiments, coefficient multipliers are adjusted until the output signal y_k ~~411~~ 441 closely approximates an expected signal.